

### DESCRIPTION:

This document describes Aplus 512M x 64-bit 4GB DDR3 SDRAM (Synchronous DRAM) Dual In-Line Memory Module. The components on this module include eight 512M x 8-bit DDR3 SDRAMs in FBGA packages and a 2048-bit serial EEPROM. Those components were mounted on a 240-pin printed circuit board. This 240-pin DIMM is used to be mounted into 240-pin edge connector sockets and data I/O transactions could be apply on both edges of DQS. The electrical and mechanical specifications are as follows:

### FEATURES:

DDR3L functionality and operations supported as defined in the component data sheet

240-pin, unbuffered dual in-line memory module

Fast data transfer rates: PC3-14900, PC3-12800, or PC3-10600

$V_{DD} = V_{DDQ} = 1.35V$  (1.238 – 1.45V)

$V_{DD} = V_{DDQ} = 1.5V$  (1.425 – 1.575V)

Backward-compatible to  $V_{DD} = V_{DDQ} = 1.5V \pm 0.075V$

$V_{DDSPD} = 3.0 - 3.6V$

Reset pin for improved system stability

Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals

Single-rank

Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)

Adjustable data-output drive strength

Serial presence-detect (SPD) EEPROM

Gold edge contacts

Halogen-free

Fly-by topology

Terminated control, command, and address bus

### Options

Operating temperature

- Commercial ( $0^{\circ}C \leq TA \leq 70^{\circ}C$ )

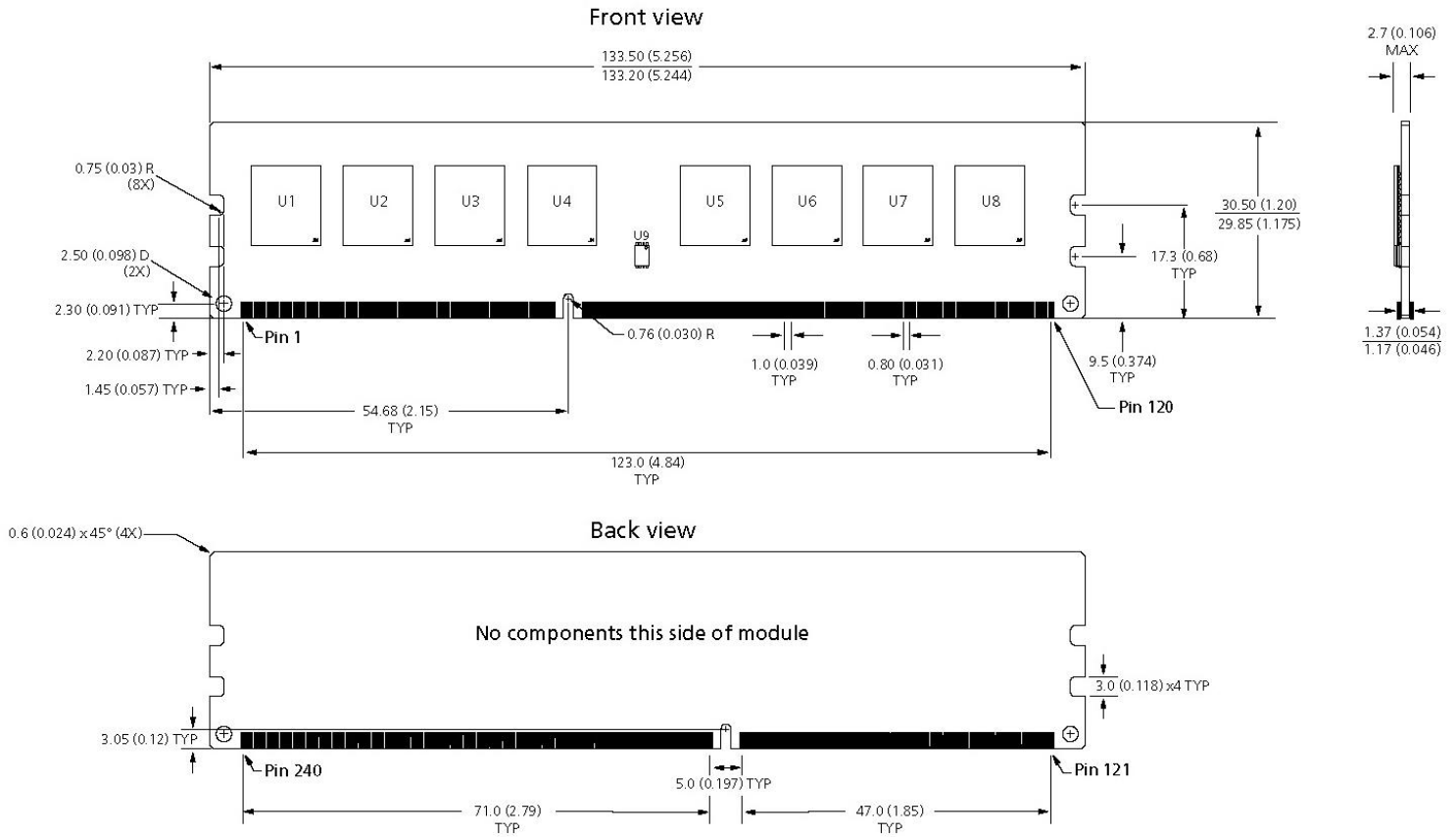
Frequency/CAS latency

- 1.07ns @ CL = 13 (DDR3-1866)

- 1.25ns @ CL = 11 (DDR3-1600)

- 1.5ns @ CL = 9 (DDR3-1333)

Industry Nomenclature	Data Rate (MT/s)				tRCD (ns)	tRP (ns)	tRC (ns)	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-tRCD-tRP)
	CL=13	CL=11	CL=10	CL=9						
PC3-14900	1866	1600	1333	1333	13.125	13.125	47.125	14.9 GB/s	1.07ns/1866 MT/s	13-13-13
PC3-12800		1600	1333	1333	13.125	13.125	48.125	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
PC3-10600			1333	1333	13.125	13.125	49.125	10.6GB/s	1.5ns/1333 MT/s	9-9-9



- Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
  2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.