1. Product Description

This defines the electrical and mechanical requirements for the memory module, a 144-pin, 32-bit wide, Unbuffered Synchronous Double Data Rate (DDR3) SDRAM 32-bit Dual In-Line Memory Module (DDR3 32b-SO-DIMM). It also defines a slower version, the using DDR3 SDRAMs. These DDR3 32b-SODIMMs are intended for use in cost sensitive, low pin count applications such as peripheral devices. examples are included which provide an 32b-SO-DIMM implementations must use the verification in the design**.**

Product Family Attributes

Attribute:	**Values:**	**Notes:**
32b-SO-DIMM Organization	x32	
32b-SO-DIMM Dimensions (nominal)	30.0 mm high, 67.60 mm wide / MO-274 variation	
32b-SO-DIMM Types Supported	Unbuffered	
Pin Count	144	
Pin pitch	0.8 mm	
SDRAMs Supported	1Gb, 2Gb, 4Gb	
Capacity	512 MB, 1 GB, 2 GB	
Serial Presence Detect	Should be consistent with JEDEC JC45	
Voltage Options, Nominal	1.5V (DDR3 / V_{DD}), 1.35V (DDR3L/V_{DD}) 3.3V V_{DD}SPD	1
Interface	SSTL_15/13.5	

Raw Card Summary

Raw Card Number of DDR SDRAMs SDRAM Organization Number of Ranks

B	4 or 8	x8	1 or 2

2. Environmental Requirements

DDR3 SDRAM Unbuffered 32b-SO-DIMMs are intended for use in computing peripheral environments that have limited capacity for heat dissipation

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	0 to +80	0C	1
HOPR	Operating Humidity (relative)	10 to 90	%	1
TSTG	Storage Temperature	-50 to +100	0C	1
HSTG	Storage Humidity (without condensation)	5 to 95	%	1
	Barometric Pressure (operating & storage)	105 to 69	kPa	1.2

1. Stressess greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.

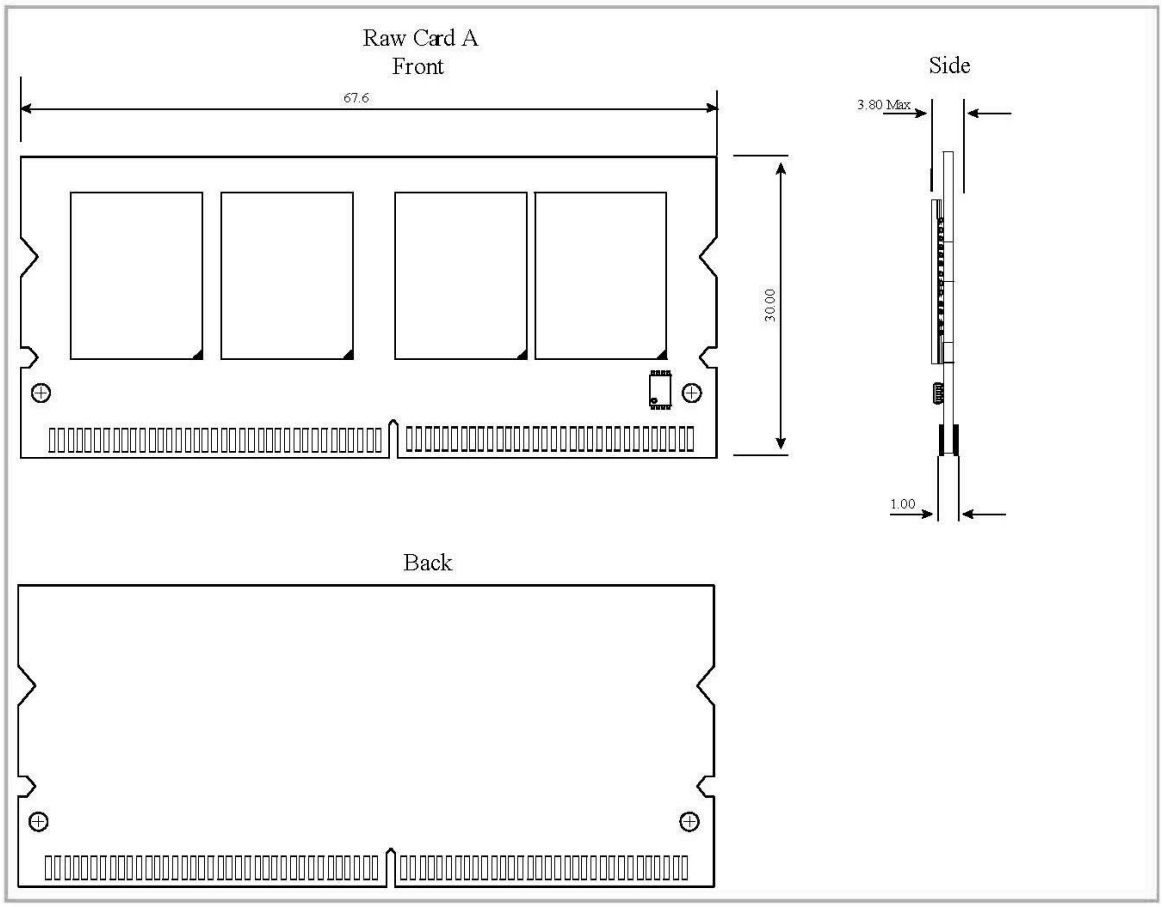
3. Architecture Pin Description

CK[1:0]	Clock Inputs, positive line	2	DQ[31:0]	Data Input/Output	32
CK[1:0]	Clock Inputs, negative line	2	DM[3:0]	Data Masks	4
CKE[1:0]	Clock Enables	2	DQS[3:0]	Data strobes positive line	4
RAS	Row Address Strobe	1	DQS[3:0]	Data strobes negative line	4
CAS	Column Address Strobe	1	TEST	Logic Analyzer specific test pin (No connect on 32b-SO-DIMM)	
WE	Write Enable	1	EVENT_n	Reserved for optional hardware temperature sensing	1
S[1:0]	Chip Selects	2	VDD	SDRAM Core and I/O Power	18
A[9:0],A11, A[13:15]	Address Inputs	14	VSS	Common Ground	26
A10/AP	Address Inputs/Autoprecharge	1	VREF	Input/Output Reference	1
A12/BC,n	Address Input / Burst chop		VDDSPD	SPD Power	
BA[2:0]	SDRAM Bank Address	3	VREFCA	VREFCA Reference Voltage for CA	1
ODT[1:0]	On-die termination	2	VREFDQ	Reference Voltage for DQ	1
SCL	Serial Presence Detect (SPD) Clock Input	1	NC	Reserved for future use	
SDA	SPD Data Input/Output	1	RESET_n	SDRAM control pin	1
SA[2:0]	SPD address	3	VTT	Termination voltage	

Total: 144

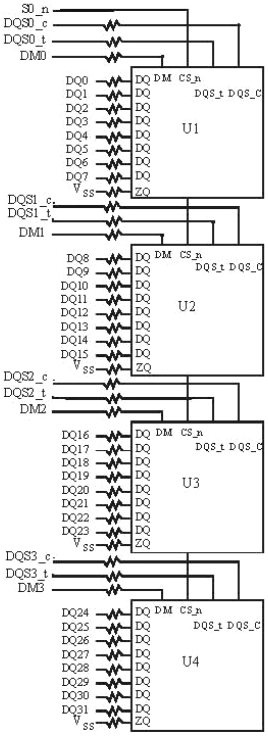
General Layout

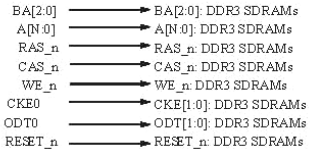
32b-SO-DIMM, populated as one physical ranks of x8 DDR3 SDRAMs

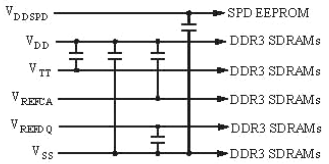


Note 1: All dimensions are typical unless otherwise stated. (Millimeters)

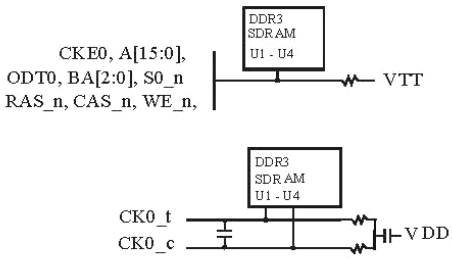
Functional Biack Diagram
DDR3 32b-SO-DIMM, popuiated as one physical ranks of x8 DDR3 SDRAMs

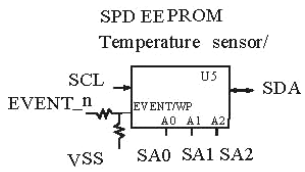






Clock, control , command, and address line terminations:





Notes:

1. ZQ resistors are 240 ohms +/- 1%.
   For all other resistor values refer to the appropriate wiring diagram.
2. A set of DQ/DQS pair/DM group can be swapped between DRAMs.
3. Either SPD or “SPD with temp sensor” can be implemented with 0ohm register option.

4. Unbuffered 32b-SO-DIMM Details

DDR 32b-SO-DIMM

Raw Card	32b-SODIMM Capacity	32b-SODIMM Organization	SDRAM Density	SDRAM Organization	# of SDRAMs	# of Ranks	SDRAM Package Type	# of banks in SDRAM	# Address bits row/col
B	512	128M x 32	1 Gbit	128 M x 8	4	1	BGA	4	14/10
B	1024	256M x 32	1 Gbit	256 M x 8	4	1	BGA	4	14/10
B	2048	512M x 32	4 Gbit	512 M x 8	4	1	BGA	4	14/10

5. 32b-SO-DIMM Mechanical Specifications

JEDEC has standardized detailed mechanical information for the 16b/32b 144 Pin SO-DIMM family. This information can be accessed on the worldwide web as follows:

Reference Simplified Mechanical Drawing with Keying Position