

## **DESCRIPTION:**

This document describes Aplus 32M x 64-bit 256MB PC100 CL2 SDRAM (Synchronous DRAM) memory module. The components on this module include eight 32M x 8-bit (4 Bank) PC100 SDRAM in TSOP packages. This 168-pin DIMM uses gold contact fingers and requires +3.3V. The electrical and mechanical specifications are as follows:

## **FEATURES:**

- Single 3.3V  $\pm$  0.3V power supply
- Burst mode operation
- Auto & self refresh capability
- LVTTTL compatible inputs and outputs
- MRS cycle with address key programs
- Latency (Access from column address)
- Burst length (1,2,4,8 & Full page)
- Data scramble (sequential & interleave)
- All inputs are sampled at the positive going edge of the system clock
- Timing Reference: CL-tRCD-tRP (2-2-2)
- Serial presence detect with EEPROM

## **PERFORMANCE:**

|                          |                            |
|--------------------------|----------------------------|
| CLK cycle time ( tCC )   | 10ns (min.) /1000ns (max.) |
| CLK to output ( tSAC )   | 6ns                        |
| Row active time ( tRAS ) | 50ns (min.) /100ns (max.)  |
| Row cycle time ( tRC )   | 70ns (min.)                |
| Power Dissipation        | 8W                         |
| Operating Temperature    | 0 °C to 70 °C              |
| Storage Temperature      | -55 °C to +150 °C          |

